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EXAMINER	
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ART UNIT	PAPER NUMBER
2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/539,111	STAIGER, DIETER E
	Examiner	Art Unit
	KRIS RHU	2184

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 5-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 5-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "disposing [of] said interface expander controllers on a single Application Specific Integrated Circuit" recited in claim 10 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Figures 2 and 3 show interface expander controllers 30A-E on different chips. Figures 4 and 5 show links to interface expander controllers 30A-E on the bottom of the figures, but that does not necessarily mean the interface expander controllers 30A-E are disposed on a single ASIC. Thus, the drawings are objected to.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Coteus et al. (US 6,202,110 B1).

Referring to claim 11, Coteus teaches an Application-Specific Integrated Circuit (ASIC) **("The memory controller 17 is made up of circuitry mounted on the backplane card 21 and mostly consists of two ASICs or application specific integrated circuits 23 and 24", column 3, lines 30-33)**, comprising: interface circuitry configured to communicate with a plurality of application-specific subsystems external to said ASIC **(note control 24 connects to I/O bus 13, figure 3)**; interface circuitry configured to communicate with a plurality of general-purpose processors external to said ASIC **(note control 24 connects to CPU bus 12, figure 3)**; and controller circuitry communicatively configured to couple each said application-specific subsystem to at least one corresponding said general-purpose processor **(control 24, figure 3)**.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (Description and Disadvantages of Prior Art), herein referred to as AAPA, with supporting evidence from Borkar et al. (US 2004/0225778 A1).

Referring to claim 1, AAPA teaches a circuit in an embedded processing system covering a number of technical applications, a number of operative functions of the number of technical applications being performed via a respective number of application-specific Electronic Control Units (ECU), the circuit comprising: a) a number of controller means **("Typically, a prior art embedded processing system covering a plurality of technical applications, the operative functions of which are performed with a respective plurality of application-specific Electronic Control Units (ECU), whereby an ECU comprises a micro-controller and/or one or more processors, and specific input/output (I/O) subsystem", Page 2, Lines 13-19)** for controlling respective application specific ECUs, each of the controller means comprising a number of application-specific support functions and L/O

subsystems; and b) a number of processor units **("Typically, a prior art embedded processing system covering a plurality of technical applications, the operative functions of which are performed with a respective plurality of application-specific Electronic Control Units (ECU), whereby an ECU comprises a micro-controller and/or one or more processors, and specific input/output (I/O) subsystem", Page 2, Lines 13-19)** each having an I/O-interface operatively connecting to a respective one of the controller means and supplying that controller means with computing power.

AAPA does not appear to explicitly teach wherein at least one of the processor units and a respective controller means are implemented on different chips.

However, at the time of the invention, it would have been obvious for one of ordinary skill in the art, having the teachings of AAPA before him or her, to modify AAPA to include wherein at least one of the processor units and a respective controller means are implemented on different chips because it merely would involve implementing an obvious alternative arrangement or choice of design known at the time of the invention that would not affect the functionality of the invention and yield predictable results. Borkar teaches a controller on a different chip from a processor as an alternative arrangement to the controller and the processor being on the same chip ("Merely as an example, system 10 may be a memory system in which controller IC0 is a memory controller (either part of a processor chip or in a different chip from the processor)", paragraph

0004, lines 9-12). Thus, a processor and a controller being on different chips is a known implementation alternative to them being on the same chip that yields predictable results.

Therefore, it would have been obvious to modify AAPA to obtain the invention as specified by the instant claim.

As to claim 7, AAPA teaches an embedded system **("Typically, a prior art embedded processing system covering a plurality of technical applications, the operative functions of which are performed with a respective plurality of application-specific Electronic Control Units (ECU), whereby an ECU comprises a micro-controller and/or one or more processors, and specific input/output (I/O) subsystem", Page 2, Lines 13-19)** having an electronic circuit according to claim 1.

Referring to claim 8, AAPA teaches a method of operating an embedded processing system comprising: controlling a number of electronic control units with a number of interface expander controllers **("Typically, a prior art embedded processing system covering a plurality of technical applications, the operative functions of which are performed with a respective plurality of application-specific Electronic Control Units (ECU), whereby an ECU comprises a micro-controller and/or one or more processors, and specific input/output (I/O) subsystem", Page 2, Lines 13-19)**; and providing computing power to said interface expander controllers with a separate number of processors **("Typically, a prior art embedded processing**

system covering a plurality of technical applications, the operative functions of which are performed with a respective plurality of application-specific Electronic Control Units (ECU), whereby an ECU comprises a micro-controller and/or one or more processors, and specific input/output (I/O) subsystem", Page 2, Lines 13-19).

AAPA does not appear to explicitly teach wherein said interface expander controllers are disposed on a separate chip from said electronic control units.

However, at the time of the invention, it would have been obvious for one of ordinary skill in the art, having the teachings of AAPA before him or her, to modify AAPA to include wherein said interface expander controllers are disposed on a separate chip from said electronic control units because it merely would involve implementing an obvious alternative arrangement or choice of design known at the time of the invention that would not affect the functionality of the invention and yield predictable results. Borkar teaches a controller on a different chip from a processor as an alternative arrangement to the controller and the processor being on the same chip ("Merely as an example, system 10 may be a memory system in which controller IC0 is a memory controller (either part of a processor chip or in a different chip from the processor)", paragraph 0004, lines 9-12). Thus, a processor and a controller being on different chips is a known implementation alternative to them being on the same chip that yields predictable results.

Therefore, it would have been obvious to modify AAPA to obtain the invention as specified by the instant claim.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Sadler (US 6,408,407 B1).

As to claim 5, AAPA does not appear to teach the circuit according to claim 1, further comprising a database storing instructions on how to handle specific errors associated with the number of processor units.

Sadler, however, teaches the circuit according to claim 1, further comprising a database **("The error handler 102 further includes a user action database 212 which includes a sequence of step by step user actions to be taken to execute each remedy scenario", Column 4, Lines 36-38)** storing instructions on how to handle specific errors associated with the number of processor units.

AAPA and Sadler are analogous arts because they both teach hardware devices and errors are common for all devices.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of AAPA and Sadler before him or her, to modify AAPA to include a database storing instructions on how to handle specific errors associated with the number of processor units, as taught by Sadler, because it merely would involve implementing a known way of handling errors in

AAPA's invention. Errors are common in hardware and software, and being able to handle errors is a known important concept.

Therefore, it would have been obvious to combine Sadler with AAPA to obtain the invention as specified in the instant claim.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Seiple (US 6,222,484 B1).

As to claim 6, AAPA does not appear to teach the circuit according to claim 1, further comprising a number of emergency controllers for continuously storing current global positioning system (GPS) coordinates and configured to send an emergency signal including the coordinates in case a number of external sensor devices detect an emergency case.

Seiple, however, teaches the circuit according to claim 1, further comprising a number of emergency controllers for continuously storing current global positioning system (GPS) coordinates **(The PELS personal unit is updated with the most current ephemeris data during a time when the person is inactive on-board the vessel by plugging it into an input module connected with the vessel's GPS system", Column 2, Lines 44-47)** and configured to send an emergency signal **("If the person falls overboard, the PELS personal unit is activated to send an emergency signal with the person's location coordinates", Column 2, Lines 49-51)** including the

coordinates in case a number of external sensor devices detect an emergency case.

AAPA and Seiple are analogous arts because both ECUs and GPS systems are known to be used in automobiles.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of AAPA and Seiple before him or her, to modify AAPA to include a number of emergency controllers for continuously storing current global positioning system (GPS) coordinates and configured to send an emergency signal including the coordinates in case a number of external sensor devices detect an emergency case, as taught by Seiple, because it merely would involve implementing a known emergency sequence for personal GPS systems into a GPS system of a car. As Applicant's specification has shown in paragraph 2 of page 2, ECUs are known to be used in embedded systems of vehicles.

Therefore, it would have been obvious to combine Seiple with AAPA to obtain the invention as specified in the instant claim.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Coteus.

As to claim 9, AAPA does not appear to teach the method of claim 8, further comprising selectively providing communication between said interface expander controllers and said processors with a General Controller Unit.

Coteus, however, teaches selectively providing communication between said interface expander controllers and said processors with a General Controller Unit **(Memory Controller 17, figure 1)**.

AAPA and Coteus are analogous arts because they both teach communication between I/O subsystems and processors.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of AAPA and Coteus before him or her, to modify AAPA to include selectively providing communication between said interface expander controllers and said processors with a General Controller Unit, as taught by Coteus, because it allows for using only one controller to provide communication between multiple processors and multiple I/O subsystems instead of using multiple controllers to provide communication between multiple processors and multiple I/O subsystems. Thus, the system can be made smaller.

Therefore, it would have been obvious to combine Coteus with AAPA to obtain the invention as specified in the instant claim.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Denso (EP 1136325 A2).

As to claim 10, AAPA does not appear to teach the method of claim 8, further comprising disposing said interface expander controllers on a single Application Specific integrated Circuit.

Denso, however, teaches the method of claim 8, further comprising disposing said interface expander controllers on a single Application Specific integrated Circuit **(Note all of the ECUs are located on the vehicle control apparatus 1, Figure 1)**.

AAPA and Denso are analogous arts because they both teach ECUs.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of AAPA and Denso before him or her, to modify AAPA to include disposing said interface expander controllers on a single Application Specific integrated Circuit, as taught by Denso, because it would merely be an alternative arrangement or choice of design that would not affect the functionality of the invention. The modification would produce similar results.

Therefore, it would have been obvious to modify AAPA to obtain the invention as specified by the instant claim.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Akai et al. (US 5,434,998).

As to claim 12, Coteus does not appear to teach the ASIC of claim 11, in which said controller circuitry is further configured to monitor at least one of said general-purpose processors or said application-specific subsystems for at least one anomaly.

Akai, however, teaches said controller circuitry being further configured to monitor at least one of said general-purpose processors or said application-

specific subsystems for at least one anomaly **("Dual control unit DXC monitors operation of processor units PC1, PC2; actuates either one (e.g. PC1) of the processor units PC1, PC2 while keeping the other (e.g. PC2) on standby; and operates the switch to assign actual operation to unit PC2 when processor unit PC1, which in an operated state fails or is demounted form the system, e.g. for maintenance work or the like", column 1, lines 26-33)**.

Coteus and Akai are analogous arts because they both teach a controller connecting to multiple processors.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Coteus and Akai before him or her, to modify Coteus to include said controller circuitry being further configured to monitor at least one of said general-purpose processors or said application-specific subsystems for at least one anomaly, as taught by Akai, because it would improve the reliability of the system.

Therefore, it would have been obvious to combine Akai with Coteus to obtain the invention as specified in the instant claim.

11. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus/Akai in view of Sadler.

As to claim 13, Coteus/Akai does not appear to teach the ASIC of claim 12, in which said controller circuitry further comprises a database storing instructions of actions to take in response to at least one specific said anomaly.

Sadler, however, teaches said controller circuitry further comprising a database **("The error handler 102 further includes a user action database 212 which includes a sequence of step by step user actions to be taken to execute each remedy scenario", Column 4, Lines 36-38)** storing instructions of actions to take in response to at least one specific said anomaly.

Coteus/Akai and Sadler are analogous arts because they both teach hardware devices and errors are common for all devices.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Coteus/Akai and Sadler before him or her, to modify Coteus/Akai to include said controller circuitry further comprising a database storing instructions of actions to take in response to at least one specific said anomaly, as taught by Sadler, because it merely would involve implementing a known way of handling errors in Coteus/Akai's invention. Errors are common in hardware and software, and being able to handle errors is a known important concept.

Therefore, it would have been obvious to combine Sadler with Coteus/Akai to obtain the invention as specified in the instant claim.

As to claim 14, Coteus/Akai teaches the ASIC of claim 13, said controller circuitry being further configured to dynamically alter said coupling of at least one application-specific subsystem to said at least one corresponding general-purpose processor in response to detecting a said anomaly **("Dual control unit DXC monitors operation of processor units PC1, PC2; actuates either one**

(e.g. PC1) of the processor units PC1, PC2 while keeping the other (e.g. PC2) on standby; and operates the switch to assign actual operation to unit PC2 when processor unit PC1, which in an operated state fails or is demounted form the system, e.g. for maintenance work or the like", column 1, lines 26-33).

As to claim 15, Coteus/Akai teaches the ASIC of claim 14, in which said anomaly comprises a breakdown in a said general-purpose processor **("Dual control unit DXC monitors operation of processor units PC1, PC2; actuates either one (e.g. PC1) of the processor units PC1, PC2 while keeping the other (e.g. PC2) on standby; and operates the switch to assign actual operation to unit PC2 when processor unit PC1, which in an operated state fails or is demounted form the system, e.g. for maintenance work or the like", column 1, lines 26-33**).

As to claim 16, Coteus/Akai teaches the ASIC of claim 15, in which said controller circuitry is configured to dynamically couple a said application-specific subsystem that was previously coupled to said general-purpose processor experiencing said breakdown to a new said general-purpose processor **("Dual control unit DXC monitors operation of processor units PC1, PC2; actuates either one (e.g. PC1) of the processor units PC1, PC2 while keeping the other (e.g. PC2) on standby; and operates the switch to assign actual operation to unit PC2 when processor unit PC1, which in an operated state**

fails or is demounted form the system, e.g. for maintenance work or the like", column 1, lines 26-33).

12. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus/Akai/Sadler in view of Barlow et al. (US 5,150,466).

As to claim 17, Coteus/Akai/Sadler does not appear to teach the ASIC of claim 16, in which said instructions comprise instructions for prioritizing said application-specific subsystems.

Barlow, however, teaches prioritizing application-specific subsystems **("It enables high performance I/O subsystems (that utilize many bus cycles) to be placed at higher positional priorities on the bus than the high priority I/O subsystems, while still allowing low performance (but high priority) I/O subsystems access to the bus when they require it", column 7, lines 16-21)**.

Coteus/Akai/Sadler and Barlow are analogous arts because they both teach I/O subsystems.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Coteus/Akai/Sadler and Barlow before him or her, to modify Coteus/Akai/Sadler to include prioritizing application-specific subsystems as taught by Barlow because it establishes an order in which I/O is performed and allows for more important I/O or I/O subsystems to be prioritized.

Therefore, it would have been obvious to combine Barlow with Coteus/Akai/Sadler to obtain the invention as specified in the instant claim.

13. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus/Akai/Sadler in view of Seiple.

As to claim 18, Coteus/Akai/Sadler does not appear to teach the ASIC device of claim 16, in which said instructions comprise instructions to wirelessly transmit a current location of said ASIC device to a recipient.

Seiple, however, teaches in which said instructions comprise instructions to wirelessly transmit a current location of said ASIC device to a recipient **("If the person falls overboard, the PELS personal unit is activated to send an emergency signal with the person's location coordinates", Column 2, Lines 49-51)**.

Coteus/Akai/Sadler and Seiple are analogous arts because both teach the use of ASICs.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Coteus/Akai/Sadler and Seiple before him or her, to modify Coteus/Akai/Sadler to include in which said instructions comprise instructions to wirelessly transmit a current location of said ASIC device to a recipient, as taught by Seiple, because it merely would involve implementing a known use of a GPS system to transmit coordinates of an ASIC.

Therefore, it would have been obvious to combine Seiple with Coteus/Akai/Sadler to obtain the invention as specified in the instant claim.

As to claim 19, Coteus/Akai/Sadler does not appear to teach the ASIC device of claim 18, further comprising transmitter circuitry for transmitting said current location of said ASIC device to said recipient.

Seiple, however, teaches transmitter circuitry for transmitting said current location of said ASIC device to said recipient **("If the person falls overboard, the PELS personal unit is activated to send an emergency signal with the person's location coordinates", Column 2, Lines 49-51)**.

Coteus/Akai/Sadler and Seiple are analogous arts because both teach the use of ASICs.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Coteus/Akai/Sadler and Seiple before him or her, to modify Coteus/Akai/Sadler to include transmitter circuitry for transmitting said current location of said ASIC device to said recipient, as taught by Seiple, because it merely would involve implementing a known use of a GPS system to transmit coordinates of an ASIC.

Therefore, it would have been obvious to combine Seiple with Coteus/Akai/Sadler to obtain the invention as specified in the instant claim.

14. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus/Akai/Sadler/Seiple in view of Takeuchi (US 5,475,269).

As to claim 20, Coteus/Akai/Sadler/Seiple does not appear to teach the ASIC device of claim 19, in which said transmitter circuitry comprises a

condenser device configured to power said transmitter circuitry if a main source of power for said ASIC device is lost.

Takeuchi, however, teaches in which said transmitter circuitry comprises a condenser device configured to power said transmitter circuitry if a main source of power for said ASIC device is lost **("The above condenser also acts as a backup power source for the use of the microcomputer", column 1, lines 51-52)**.

Coteus/Akai/Sadler/Seiple and Takeuchi are analogous arts because they both teach devices that require power.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Coteus/Akai/Sadler/Seiple and Takeuchi before him or her, to modify Coteus/Akai/Sadler/Seiple to include in which said transmitter circuitry comprises a condenser device configured to power said transmitter circuitry if a main source of power for said ASIC device is lost, as taught by Takeuchi, because it would prevent or reduce downtime.

Therefore, it would have been obvious to combine Takeuchi with Coteus/Akai/Sadler/Seiple to obtain the invention as specified in the instant claim.

Allowable Subject Matter

15. Claim 2 is allowable over prior art.

16. The following is a statement of reasons for the indication of allowable subject matter: The prior arts do not teach or fairly suggest the following limitations in claim 2:

> mapping means for mapping the I/O subsystems to the processor units, and a General Controller Unit operatively coupled to the mapping means and configured to dynamically switch at least one of the processor units into communication with a selected controller means based on processor timing requirements.

Further the combination of the above limitations with all of the other limitations in the respective independent claim is not obvious.

Response to Arguments

17. Applicant's arguments filed 1/4/11 have been fully considered but they are not persuasive.

18. Regarding the objection to the drawings, Applicant's argued, "**Fig. 10 shows a block diagram including of a system having logic (66) to interface with and control multiple external electronic control units (30A-30E) and multiple external generic CPUs (40). (Specification, Fig. 10 and pp. 11-12). Thus, each subsystem of physical logic for interfacing with and controlling a separate electronic control unit taught in Fig. 5 reads on an 'interface expander controller' recited in independent claim 8 and dependent claim 10. Additionally, the specification teaches that '[a]ll logic detailed in fig. 5 or fig. 4 may be advantageously provided**

in form of a programmable ASIC, or a static ASIC.' (Specification, p. 11 lines 1-2). Taken in this context, Fig. 5 plainly shows a single ASIC that embodies multiple interface expander controllers within the scope of claim 10. Consequently, the objection to the drawings is improper and should be reconsidered and withdraw", in lines 6-15 on page 8. Applicant's arguments are not persuasive. Examiner will assume that the Applicant was meaning to refer to figure 5 when stating "Fig. 10" because figure 10 does not exist. Note the specification recites, "a physical interface logic 66 having respective input registers 88 which provides for the physical access to the actual application-specific I/O systems (CAN-bus, mobile phone and other I/O)", in the last 4 lines on page 11. The specification further recites, "for each ECU a specialised, application-specific interface chip 30 A, 30 B, ... 30 E is provided" in lines 5-6 on page 8. The specification also recites, "a plurality of extracted interfaces – hereafter called interface expander controllers ... comprising each a respective one of said application-specific I/O subsystems", lines 6-10 on page 4. Thus, modules 30A-E are interface expander controllers, not electronic control units. The physical interface logic 66, therefore, do not comprise expander controllers 30A-30E because it links to application-specific I/O systems CAN-B, CAN-C, etc., otherwise known as application-specific interface chips 30A-30E.

19. Regarding claim 1, Applicant argued that the limitation, "wherein at least one of the processor units and a respective controller means are implemented on different chips", is not an obvious design choice, and cites several BPAI cases to support the argument. Applicant's argument is not persuasive. As shown in the above rejection,

supporting art is provided to show that providing processors and controllers on different chips was, at the time of the invention, a known alternative arrangement to providing them on the same chip, and, therefore, is an obvious implementation. Borkar teaches these two arrangements *in the alternative*. See "Merely as an example, system 10 may be a memory system in which controller IC0 is a memory controller (*either part of a processor chip or in a different chip from the processor*)" in paragraph 0004, lines 9-12 (emphasis added). Therefore, implementing a processor and a controller on different chips is an obvious implementation because it is a known alternative arrangement to implementing them on the same chip. Similar arguments were made regarding claim 8.

20. Regarding claim 9, though the limitations in the claim were indicated as allowable subject matter in the previous office action, new art was found that reads on the claim. New grounds of rejection have been made.

/Henry W.H. Tsai/

Supervisory Patent Examiner, Art Unit 2184